ABSTRACT

A distributed interface between a microprocessor, or a standard bus, and user macro-cells belonging to an ASIC, or FPGA, or similar silicon devices is disclosed. The interface consists of a main module connected to the microprocessor bus, at one side, and to a COMMON-BUS inside the interface on which a cluster of peripheral modules is appended, at the other side. Peripheral modules are further connected to the user macro-cells through as many point-to-point buses as the implemented macro-cells, in order to transfer signals in the two directions. A set of hardware and firmware resources comprehensive of the most popular needs of the user macro-cells, like: registers, counters, synchronizers, dual port memories both of RAM and FIFO type either synchronous or asynchronous with respect to macro-cells clock, etc., is encompassed in each peripheral module. Subsets of the standardizable resources are diversely configurable in each peripheral module in accordance with specific needs of respective interconnected user macro-cells (**Figure 9**).

The implemented communication protocol between the main module and the peripheral modules overcomes the limitations of "classic" interfaces when not prefetchable resources are interfaces to peripheral modules.